HAKSUN LEE

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Education

Georgia Institute of Technology, Atlanta, GA
Ph.D candidate in Electrical Engineering 01/2016 – present

Georgia Institute of Technology, Atlanta, GA
M.S. in Electrical Engineering 08/2012

Purdue University, West Lafayette, IN
B.S. in Electrical Engineering 12/2010

Research and Professional Experience

Graduate Research Assistant 2016 – present
Georgia Institute of Technology
Research advisor: Professor. Rao Tummala
- Design and demonstration of ultra-low parasitic and 3D high-power module using WBG devices for automotive application.

Researcher 2012 – 2015
Electronics and Telecommunications Research Institute (ETRI)
Project manager: Dr. Kwang-Seong Choi
- Development of TSV multi-die stacking process.
- Reliability analysis of low temperature interconnection for flexible substrates.
- 3D transmit/receive module integration based on Si interposer technology.
- Characterization and optimization of novel bumping and underfill materials.

Honors and Awards

Best Student Paper – FUTURECAR: New Era of Automotive Electronics Workshop, Atlanta, GA 2016

Publications and Presentations

Journals

- **H. Lee,** V. Smet and R. Tummala, "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 239-255, March 2020.
- **H. Lee**, K.-S. Choi, Y.-S. Eom, H.-C. Bae, and J. H. Lee, "Sn58Bi Solder Interconnection for Low Temperature Flex-on-Flex Bonding," ETRI Journal, vol. 38, no. 6, pp.1163-1171, Dec. 2016.

- J. Son, Y.-S. Eom, K.-S. Choi, **H. Lee**, H.-C. Bae, and J.-H. Lee, "HV-SoP Technology for Maskless Fine-Pitch Bumping Process," ETRI Journal, vol. 37, no. 3, pp. 523-532, Jun. 2015.
- Kwang-Seong Choi, **H. Lee**, Hyun-Cheol Bae, Yong-Sung Eom, and Jin Ho Lee, "Interconnection Technology Based on InSn Solder for Flexible Display Applications," ETRI Journal, vol. 37, no. 2, pp. 387-394, Apr. 2015.
- **H. Lee**, Y.-S. Eom, H.-C. Bae, K.-S. Choi, and J. H. Lee, "Characterization and Estimation of Solder-on-Pad Process for Fine-Pitch Applications." IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 4, No 10, pp. 1729 – 1738, Oct. 2014.
- Y.-S. Eom, J.-H. Son, K.-S. Jang, **H.-S Lee**, H.-C. Bae, K.-S. Choi, and H.-S. Choi. "Characterization of Fluxing and Hybrid Underfills with Micro-encapsulated Catalyst for Long Pot Life." ETRI Journal, Vol. 36, No. 3, pp. 343–351, Jun. 2014.
- H.-C. Bae, **H. Lee**, K.-S. Choi, and Y.-S. Eom, "Fine-pitch solder on pad process for microbump interconnection." ETRI Journal, vol. 35, no. 6, pp. 1152–1155, Dec. 2013.

Conference Proceedings

- **H. Lee**, V. Smet, P. M. Raj and R. Tummala, "Design of Low-Profile Integrated Transformer and Inductor for Substrate-Embedding in 1-5kW Isolated GaN DC-DC Converters," Electronic Components and Technology Conference (ECTC), FL, USA, May. 2017.
- K.-S. Choi, **H. Lee**, H.-C. Bae, Y.-S. Eom, K. Lee, T. Fukushima, M. Koyanagi, and J.H. Lee "Characterization of 3D Stacked High Resistivity Si Interposers with Polymer TSV liners for 3D RF Module." Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, May. 2015.
- **H. Lee**, Y.-S. Eom, H.-C. Bae, K.-S. Choi, and J. H. Lee "Development of Low Contact Resistance Interconnection for Display Applications." Electronics System-Integration Conference (ESTC), Helsinki, Finland, Sep. 2014. *(Oral Presentation)*
- Y.-S. Eom, **H.-S. Lee**, H.-C. Bae, and K.-S. Choi "Flip-Chip Bonding Processes with Low Volume SoP Technology." Electronics System-Integration Conference (ESTC), Helsinki, Finland, Sep. 2014.
- K.-S. Choi, **H. Lee**, H.-C. Bae, Y.-S. Eom, "Maskless Screen Printing Technology for 20μm-Pitch, 52InSn Solder Interconnections in Display Applications." Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, May. 2014.
- K.-S. Choi, H.-E. Bae, **H. Lee**, H.-C. Bae, Y.-S. Eom, "Thermally Activated Bumping Process using Sn3.0Ag0.5Cu Solder Powder for Low-Cost Interposers." 46th International Symposium on Microelectronics (IMAPS), Orlando, FL, USA, Sep. 2013.
- **H. Lee**, Y.-S. Eom, H.-C. Bae, and K.-S. Choi, "Novel interconnection technology for flex-on-glass (FOG) applications." European Microelectronics Packaging Conference (EMPC), Grenoble, France, Sep. 2013. *(Poster Presentation)*
- H.-C. Bae, **H. Lee,** Y.-S. Eom, and K.-S. Choi. "Novel Low-volume solder-on-pad for fine pitch Cu pillar bump." European Microelectronics Packaging Conference (EMPC), Grenoble, France, Sep. 2013. **Best Poster Award**
- J. V. Clark, F. Li, **H. Lee**, K. Kadasia. "Using MEMS as Self-Calibrating Force-Displacement Transducers: A Theoretical Study". Nanotech Conference & Expo, Anaheim, CA, USA, Jun. 2010.

Presentations

- **H. Lee** et al., “3D TSV Chip Stacking Process Using Solder-on-Pad Technology.” Annual Summer Conference of the Korean Institute of Electrical and Electronic Material Engineers (KIEEME), Sokcho, South Korea, Jun. 2014. *(Poster Presentation)*
- **H. Lee**, J. V. Clark. “Thermally Induced-Noise Reduction Using an Electrostatic Force Feedback.” COMSOL Conference, Boston MA, USA. Oct. 2010 *(Oral Presentation)*

Patents and Patent Applications

- KS Choi, HC Bae, **H Lee**, YS Eom, “Bonding structure of electronic equipment”, 2017, U.S. Patent No. 9538666
- KS Choi, YS Eom, HC Bae, **H Lee**, “Methods of forming bump and semiconductor device with the same”, 2015, U.S. Patent No. 9006037
- **H Lee**, KS Choi, YS Eom, HC Bae, “Semiconductor package and method for manufacturing the same”, 2016, U.S. Patent Application No. 15/172097
- HC Bae, YS Eom, **H Lee**, KS Choi, “Transceiver module and communication apparatus including the same”, 2015, U.S. Patent Application No. 14/857818
- KS Choi, HC Bae, YS Eom, JH Lee, **H Lee**, “Method of fabricating a semiconductor package”, 2015, U.S. Patent Application No. 14/958341
- KS Choi, HC Bae, YS Eom, **H Lee** “Stack module package and method for manufacturing the same”, 2015, U.S. Patent Application No. 14/685400
- HC Bae, YS Eom, KS Choi, **H Lee** “Method of fabricating a solder particle”, 2014, U.S. Patent Application No. 14/089442
- **H Lee**, KS Choi, YS Eom, HC Bae, “Semiconductor device and method of manufacturing the same”, 2014, U.S. Patent Application No. 14/338050

Relevant Skills

Packaging Equipment
- SMT reflow machine
- Flip-chip bonder (Laurier M9, Finetech Fineplacer)
- Wire bonder (Kulicke & Soffa)

Material Characterization Equipment
- Dynamic Scanning Calorimetry (TA Instruments)
- Thermal Gravimetric Analysis (TA Instruments)
- Rheometer (HAAKE MARS)

Fabrication Equipment
- RF/DC sputter
- Thermal evaporator

Simulation Tools
- COMSOL Multi-physics
- MATLAB Simulink
- LTSPICE
- ANSYS
- SolidWorks