TAILONG SHI

3D Systems Packaging Research Center
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EDUCATION

Georgia Institute of Technology, Atlanta, Georgia, USA 08/2014 - present
Doctor of Philosophy in Electrical and Computer Engineering,

Santa Clara University, Santa Clara, California, USA 09/2012 - 06/2014
Master of Science in Electrical Engineering, GPA: 3.87/4.0

Southeast University, Nanjing, China 08/2008 - 06/2012
Bachelor of Engineering in Information Engineering, GPA: 83.1/100

RESEARCH EXPERIENCE

Georgia Institute of Technology, Atlanta, Georgia, USA
Graduate Research Assistant in 3D Systems Packaging Research Center

Project: 2D Ultra-thin Glass Mobile BGA Package 2014 - 2016

- Designed and demonstrated a four-metal layer 140 μm thick fully-integrated single-chip glass BGA package at 40/80 μm off-chip I/O pitch with through-package vias (TPVs) at 160 μm pitch for mobile applications.
  - Designed nine types of multi-level test structures to evaluate the yield at each fabrication process step, including through-package vias daisy chains, micro-vias daisy chains, chip-level interconnection daisy chains, and other multi-layer test structures.
  - Designed each layer's layout of the fully-integrated package using AutoCAD, including the through package vias layer, four metal layers, two micro-vias layers, and two passivation layers. Panelized the 15mm x 15mm coupon design to fit in a 150mm x 150mm panel with alignment mark design on each layer.
  - Fabricated the four layer fully-integrated glass package on 100 μm thick low coefficient of thermal expansion (CTE) glass panels with 160 μm pitch through-package vias (TPVs), using advanced semi-additive process (SAP) for multilayer RDLs and micro-vias.
  - Achieved over 99% TPV yield at 160μm pitch by advanced via-first processes with plasma etching primer opening method.
  - Demonstrated chip-level assembly by standard Cu pillar thermos-compression bonding (TCB) process on substrate strips at 40/80 μm off-chip I/O pitch.
  - Demonstrated for the first time the DC signal transmission from the die at 40/80μm I/O pitch, through a 100μm-thick glass package with TPVs and multilayered wiring, to the board and back.

Project: Glass Panel Embedding Package 2016 - 2018

- Demonstrated for first time an ultra-thin, panel-level glass fan-out package to serve as the next generation of fan-out packaging for high density digital and high performance analog, power, RF and mm-wave applications.
  - Designed and demonstrated an ultra-thin panel-level glass fan-out package with total thickness less than 215 μm, including 50 μm thick glass carrier, 70 μm thick glass cavity panel, 75 μm thick test chips embedded in the glass cavity, bonding dry film and the double-side RDL layers.
  - Process development and optimization including glass-to-glass bonding, die placement into glass cavity, surface planarization and chip-package microvia laser drilling.
  - Proposed 77GHz Radar Module with advanced panel-level glass fan-out structure.
  - Modeled chip-to-package interconnection loss of the panel-level glass fan-out architecture for high frequency applications.

SKILLS

Software: AutoCAD, HFSS, SONNET, Keysight ADS, CAM, MATLAB

MAJOR PUBLICATIONS

T. Shi *et al*., "Design, Demonstration and Characterization of Ultra-Thin Low-Warpage Glass BGA Packages for Smart Mobile Application Processor," in *66th IEEE Electronic Components and Technology Conference, (ECTC) 2016*, May 31, 2016 - June 3, 2016, Las Vegas, NV, United States, 2016, pp. 1465-1470

T. Shi *et al*., "First Demonstration of Panel Glass Fan-Out (GFO) Packages for High I/O Density and High Frequency Multi-chip Integration," *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 41-46.

T. Shi *et al*., " Next Generation of Automotive Radar with Leading-edge Advances in SiGe Devices and Glass Panel Embedding Packaging," accepted in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC).*

T. Shi *et al*., "Tracing vocal fold vibrations using level set segmentation method," *International journal for numerical methods in biomedical engineering* 31.6 (2015).