Xiaofan Jia

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Summary

Working on wireless communication, RF waveguide integration and the miniaturization of RF components.

Familiar with microstrip filter design, D-band dielectric waveguide design, D-band measurement.

Education

Georgia Institute of Technology *Aug. 2019 - Present*
Ph.D. Student, Graduate Research Assistant
Advisor: Prof. Madhavan Swaminathan
Overall GPA: 3.75/4.0
School of Electrical and Computer Engineering

Tianjin University *Sept. 2015 - July. 2019*
Major in Integrated Circuit Design and Integrated System
Overall GPA: 3.87/4.0

Technical Skills

EDA Tools: ADS, Ansys HFSS, Cadence, HSpice, ModelSim, Altium Designer

Programming Languages: Python, Matlab, Verilog, C, C++, PHP, HTML, SQL

Projects

High Bandwidth and Low Insertion Loss Interconnections at D-Band *Jan. 2020 - Present*
Focus on SIW, Dielectric waveguide and Microstrip line. Trying to find high bandwidth, low loss, low cross talk and high power handling interconnections for the next generation communication systems.

D-Band Microstrip Hairpin Bandpass Filter on Glass Stack-up *Sept. 2019 - Jan. 2020*
Realized a 3rd order package-integrated and ultra-thin hairpin bandpass filter (BPF) working in D-Band on glass stack-up with size smaller than $0.9\lambda_0$ x $0.5\lambda_0$. The passband insertion loss is less than 4dB between 135 GHz - 148 GHz.

Research on Low Phase Noise VCO Based on SISL Technology *Sept. 2018 - May. 2019*
Undergraduate final project. Using ADS and HFSS simulation tools, designed a low phase noise voltage-controlled oscillator (VCO) based on substrate-integrated suspended line (SISL) technology.

Research on CMOS Voltage-Controlled Oscillator *Mar. 2018 - Sept. 2018*
Learned basic principles of VCO and phase noise models. Using Cadence Virtuoso, designed cross-coupled VCO with tuning range 29 - 33GHz and simulated phase noise around -120dBc/Hz@10MHz using GLOBALFOUNDRIES 55nm PDK.

Research on Flexible Single Crystal Semiconductor Transistor *May. 2017 - Apr. 2018*
Modeling of bending characteristics for flexible transistors, searching for reliable models for high-performance flexible MOSFET on PET substrate. Mainly responsible for designing the layout of flexible transistors and fitting characteristic curve of the new transistor model.

Research on Self-Tracing Car Based on CMOS Camera Sensor *Oct. 2016 - Apr. 2017*

Mainly responsible for designing the motherboard (including voltage regulator circuits and peripheral circuits for MCU), detecting track from image data and implementing part of the PID control algorithm.

Online Learning Platform *Sept. 2015 - Oct. 2016*

Finished scripts of an online learning platform for students at Tianjin University using PHP scripting language and MySQL database.